SHORT COURSE ON



Modeling, Simulation and Characterization of Nano-Transistors



OCTOBER 26 - 30, 2015

Organized by Department of Electrical Engineering, IIT Kanpur



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Website http://www.iitk.ac.in/nanolab/sc

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Registration Fee**

Faculty: Rs. 12,000 Industry/R&D Labs: Rs. 15,000 Students: Rs. 5,000

Coordinators

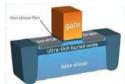
Dr. Y. S. Chauhan, IIT Kanpur Dr. A. Agarwal, IIT Kanpur Dr. N. Mohapatra, IIT Gandhinagar

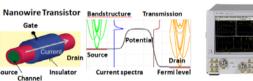
Contact

nanolab.iitk@qmail.com

Topics:

- VLSI design and Nanoelectronics
- Physics and Operation of MOSFET
- SPICE and Circuit simulation
- TCAD simulation: Theory and demonstration
- Compact Modeling: Theory and demonstration
- Scaling and Moore's Law
- International Technology Roadmap for Semiconductors
- Nanoscale Transistors: FinFET and FDSOI
- Characterization: Current and capacitance measurement •
- **RF CMOS and GaN High Electron Mobility Transistors**





Also included:

- Laboratory visits and RF transistor measurement
- New research problems in Nanoelectronics

Target Audience:

Faculty members, practicing engineers & students.

SPEAKERS









A. Dutta Dept. of EE IIT Kanpur

Y. S. Chauhan B. Mazhari Dept. of EE Dept. of EE **IIT Kanpur** IIT Kanpur

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**Registration Fee includes course fee, accommodation, food, printed lecture notes and stationery.

